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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,093	07/06/2001	Michael O. Thompson	3672-0121P	2736

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EXAMINER
HUR, JUNG H

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No. 09/899,093	Applicant(s) THOMPSON ET AL.	
	Examiner Jung (John) Hur	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17 and 18* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 08 October 2002. The changes disclosed therein was considered.

2. Claims 1-18 are pending.

Drawings

3. The corrected or substitute drawings were received on 08 October 2002. These drawings are acceptable.

Specification

4. A substitute specification filed under 37 CFR 1.125(a) must only contain subject matter from the original specification and any previously entered amendment under 37 CFR 1.121. If the substitute specification contains additional subject matter not of record, the substitute specification must be filed under 37 CFR 1.125(b) and must be accompanied by: 1) a statement that the substitute specification contains no new matter; and 2) a marked-up copy showing the amendments to be made via the substitute specification relative to the specification at the time the substitute specification is filed.

The substitute specification filed 08 October 2002 has not been entered because it does not conform to 37 CFR 1.125(b) because it was not accompanied by a statement that the substitute specification contains no new matter.

5. The amendment filed 08 October 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

On page 10, line 19 through page 12, line 20 of the substitute specification, applicant cites a new reference which was not described in the original specification as filed, and which was used for the prior rejection in the previous Office Action.

Applicant is required to cancel the new matter in the reply to this Office Action.

Priority

6. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Norway on 07 July 2000. It is noted, however, that applicant has not filed a certified copy of the 20003508 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-3, 11-14, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda (U.S. Pat. No. 5,550,770).

Regarding claims 1-3 and 17, Kuroda discloses, in Figs. 1-15 and respective portions of the specification, a memory array of cells comprising ferroelectric capacitors and a method of driving said memory array of cells, wherein all word lines and bit lines (data lines, in the reference) are controlled with a plurality of pre-defined potential levels in a predetermined, time-coordinated sequence. Kuroda further discloses read, refresh (rewrite, in the reference) and write cycles in the predetermined, time-coordinated sequence; during the read cycle, potential on a selected bit line floats in response to flowing charges when the charges are sensed (Fig. 15), and during the write or refresh cycle, the word line and bit line potentials are clamped to said sequence of potentials (Figs. 12-14). Kuroda further discloses, in Figs. 9, 10 and 12-15, three potential levels for word lines and bit lines (data lines, in the reference), such that voltage across unselected cells is about $V_S/2$ ($V_0/2$, in the reference), where V_S is defined on page 10, lines 20-27 in the instant specification. Further, Kuroda in Figs. 2-8 discloses a matrix of ferroelectric cells on a single array layer (one block of cells) wherein all memory locations (for example, C0) are accessed solely by each cell's bit line (for example, d0 for C0) and word line (for example, W00 for C0), such that the cells (C0-C7 and others in the figures), word lines (W00-W07), and bit lines (d0-d7) comprise a passive matrix.

Regarding claims 11-14 and 17, Kuroda discloses same quiescent potentials on all the word lines and bit lines (data lines, in the reference), namely, $V_0/2$ in Figs. 9 and 10, and 0 V in Figs. 12-15, where $V_0/2$ is same as the potential on unselected word lines and bit lines, and 0 V represents system ground (Figs. 2-8). In Fig. 10(C), Kuroda further discloses a precharge period where the potential on a selected bit line is changed from a quiescent potential before a floating period in which the flowing charge is sensed (precharge of data line and sense steps, in the

reference). In Fig. 15, Kuroda further discloses a precharge pulse on unselected word lines as an option, such that said precharge pulse terminates when the potential on a selected bit line changes for a read cycle. With the precharge pulse, the voltage across unselected cells on the selected bit line would be about $V_0/2$ from the onset of the precharge pulse until the read cycle is completed.

Regarding claim 18, Kuroda discloses in Figs. 9 and 10 the intervals between succeeding and following voltage levels in the voltage pulsing protocol having the same values, and the potential difference between active voltage levels is Vs or higher (Vo for WRITE and SENSE portions in Figs. 9 and 10).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,550,770) in view of Tannas (U.S. Pat. No. 4,169,258).

Regarding claim 4, Kuroda discloses a method of driving a ferroelectric memory array as in claim 1 (see above). However, Kuroda does not disclose four (4) potential levels for word lines and bit lines. Tannas discloses, in Figs. 3a-3d, four potential levels for driving a ferroelectric matrix, such that the voltage across unselected cells do not significantly exceed $V_S/3$, for the purpose of minimizing hysteresis creep and preventing undesirable hysteresis

switching. Therefore, in view of Tannas, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kuroda to use four potential levels of Tannas for the purpose of minimizing hysteresis creep and preventing undesirable hysteresis switching.

Regarding claims 6-10, Kuroda discloses a method of driving a ferroelectric memory array as in claim 1 (see above). Kuroda further discloses that the voltage across unselected cells is about one half of applied voltage across a selected cell. However, Kuroda does not disclose details of any deviation of voltages across unselected cells nor details of any deviation of potentials on word lines and bit lines. Tannas, in the specification, discloses that potentials on word lines (x-lines, in the reference) and bit lines (y-lines, in the reference) may shift either negatively or positively. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to increase the voltage across unselected cells along a selected word line by a controlled voltage and to decrease the voltage across unselected cells along a selected bit line by the same controlled voltage, or to increase the potential of unselected word lines by a controlled voltage and to decrease the potential of unselected bit lines by the same controlled voltage, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum value of a result effective variable involves only routing skill in the art. *In re Aller*, 105 USPQ 233.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,550,770) in view of Anderson (U.S. Pat. No. 3,002,182).

Regarding claim 5, Kuroda discloses a method of driving a ferroelectric memory array as in claim 1 (see above). However, Kuroda does not disclose five potential levels, of which any set of three are for word lines and any other set of three are for bit lines. Anderson discloses, in Fig. 4, for the purpose of reducing the effect of disturbing pulses on unselected cells, three potential levels for word lines (rows, in the reference) and three potential levels for bit lines (columns, in the reference) with a total of five distinct potential levels for operating a ferroelectric matrix, such that the voltage across unselected cells do not significantly exceed $V_S/3$. Therefore, in view of Anderson, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method of Kuroda to use five potentials levels of Anderson for the purpose of reducing the effect of disturbing pulses on unselected cells.

Allowable Subject Matter

12. Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior arts of record do not disclose or suggest a method of applying a pre-read reference cycle which precedes a read cycle by a selected time, wherein a signal obtained during the pre-read reference cycle is subtracted from a signal obtained during the read cycle.

Response to Arguments

13. Applicant's arguments filed 08 October 2002 have been fully considered but they are not persuasive.

On page 16, lines 10-12, applicant argues that Kuroda fails to suggest three or four levels being used for passive memory type, and on page 17, lines 7-11, Kuroda fails to access all memory locations solely by it's bit and word line on a single array layer (which is also recited in claim 1), and therefore Kuroda fails to anticipate applicants' claimed invention.

However, Kuroda in Fig. 2 discloses a matrix of ferroelectric cells on a single array layer (one block of cells) wherein all memory locations (for example, C0) are accessed solely by each cell's bit line (for example, d0 for C0) and word line (for example, W00 for C0), such that the cells (for example, C0-C7), word lines (W00-W07), and bit lines (D0-D7) comprises a passive matrix. Therefore, Kuroda anticipates applicants' claimed invention.

On page 16, lines 16-23, applicant argues that the present invention allows for permanent application of quiescent voltage to all bit and word lines, and that there is no need for applying-block-selecting voltage.

However, the limitation of permanent application of quiescent voltage is not recited in claims 11-14, and Kuroda in Figs. 9 and 10 discloses a quiescent voltage of Vo/2 for a selected matrix (selected block) before and after read/write cycles.

On page 17, lines 14-17, applicant argues that Tannas teaches that all memory cells shall initially have the same polarization magnitude and direction, and therefore does not make up the deficiencies of Kurado.

However, claims 4 and 6-10 to which Tannas is applied do not recite the requirement that such limitation be present or absent. Therefore, Tannas does make up the deficiencies of Kurado.

On page 17, line 20 through page 18, line 5, applicant argues that Anderson uses a mix of one-quarter and one-third voltage selection schemes with at least six potential levels, and therefore, is contrary to applicant's invention.

However, Andersen discloses 2Vs/3 and 3Vs/4 merely as a range of voltage for pulse 51 in Fig. 4, method of operation B, and likewise, Vs/4 and Vs/3 as a range of voltage for pulses 57, 58, and 60-61 (see column 8, lines 1-32). Therefore, it is within the skill of a person having ordinary skill in the art to select a voltage from the ranges for operation and implement in the device of Kuroda, and have $n_{WORD}=3$ (namely, for example, –Vs, 0, and +2Vs/3) and $n_{BIT}=3$ (namely, for example, –Vs/3, 0, and +Vs/3) such that n=5 (namely, –Vs, –Vs/3, 0, +Vs/3, and +2Vs/3), as cited in claim 5 to which Anderson is applied.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (703) 308-1624. The examiner can normally be reached on M-F 6:00 AM - 2:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jhh
December 9, 2002

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800